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CDB5394
CDB5396/7

Evaluation Board for CS5394 and CS5396/7

Features

- Demonstrates recommended layout and grounding arrangements
- CS8404A generates AES/EBU and/or IEC 958 compatible digital audio
- Buffered serial output interface
- Digital and analog patch areas
- On-board or externally supplied system timing

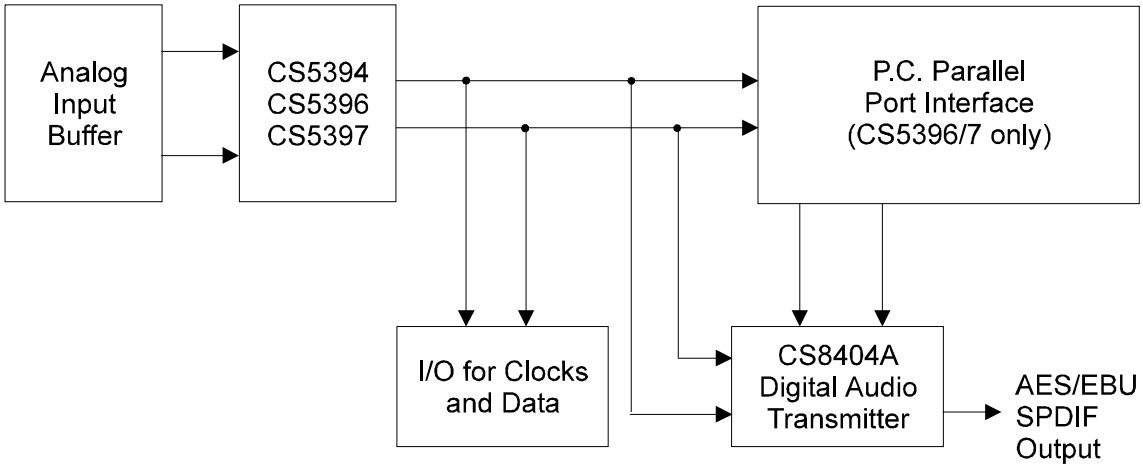
General Description

The CDB5394, CDB5396 and CDB5397 evaluation boards are an excellent means for quickly evaluating the CS5394, CS5396 and CS5397 24-bit, stereo A/D converters. Evaluation requires a digital signal processor, a low distortion analog signal source and a power supply. Analog inputs are provided via XLR connectors for both channels.

Also included is a CS8404A digital audio interface transmitter which generates AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The digital audio data is available via RCA phono and optical connectors.

The evaluation board may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION:
CDB5394, CDB5396, CDB5397



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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OVERVIEW

CDB5394/96/97 System

The CDB5394/96/97 evaluation boards are an excellent means of quickly evaluating the CS5394, CS5396 or CS5397. The CS8404A digital audio interface transmitter provides an easy interface to digital audio signal processors, including the majority of digital audio test equipment. The evaluation board has been designed to accept an analog input and provide optical and coaxial digital outputs. The evaluation board also allows the user to access clocks and data through a 10-pin header for system development.

The CDB5394/96/97 schematic has been partitioned into 7 schematics shown in Figures 2 through 8. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the connections between the partitioned schematics.

Power Supply Circuitry and Grounding

Power is supplied to the evaluation board by six binding posts as shown in Figure 8. +5VA provides 5 Volt power to the converter, VCOM buffer and the crystal oscillator. The +/-12V binding posts provide power to the analog input buffer. +5VD supplies 5 Volt power to the digital section of the board. Z1-Z4 are transient suppression diodes which also provide protection from incorrectly connected power supply leads.

Configuration for Stand-Alone or Control Port Mode

Refer to Tables 2-4 for the jumper settings required to configure the evaluation board.

Power-Down and Calibration - Stand alone Mode

The CS5394 and CS5396/97 in Stand-Alone mode are placed into the power-down mode simply by depressing the PDN switch (S1). Power-down is released when the PDN switch is released. A calibration sequence should be manually initiated by depressing the CAL switch (S2) following power-down.

Power-Down and Calibration - Control Port Mode for CDB5396/97 Only

Power-down and calibration are available only through the control port. The calibration and power-down buttons on the evaluation board are ignored when configured in the Control Port mode.

Supplied Control Port Commands for CDB5396/97

The evaluation board includes a set of DOS files which allow communication through a PC parallel port to the evaluation board.

The supplied commands include:

cal64x.bat - Performs a calibration and initialization sequence and sets the CS5396/97 into the 64X oversampling mode.

cal128x.bat - Performs a calibration and initialization sequence and sets the CS5396/97 into the 128X oversampling mode.

rdi2c.exe <Map>- This routine returns the value located in the register pointed to by <map>. The <map> value is in hex and the value returned is in hex.

wri2c.exe <map> <data> - This routine writes the value of <data> into the register pointed to by <map>. Both values are in hex.

rst.exe - Sends a reset command to the device.

mode128x.bat - Sets the device into the 128X oversampling mode. The cal128x.bat command includes this sequence.

mode64x.bat - Sets the device into the 64X oversampling mode. The cal64x.bat command includes this sequence.

gnd.bat - Disconnects the analog modulators from the input pins and attaches the modulator inputs to the internal common mode voltage.

ungnd.bat - Disconnects the analog modulators from the internal common mode voltage and attaches the modulator inputs to the input pins.

General Comments on the Parallel Port

The evaluation board will be partially powered through the PC cable when the supplies to the evaluation board are off. This will affect the RC timing circuit which places the CS5396/97 into the Control Port mode. It is required that the evaluation board go through the power-up sequence without the cable to the PC connected.

Input Buffer

The differential input circuit shown in Figure 4 is well-suited for the CS5394/96/7 in professional applications. The circuit will accept a differential or single-ended signal of either polarity and provide a differential signal with the proper DC offset to the CS5394 or CS5396/97. The circuit also incorporates 6 dB of attenuation to scale down professional input levels to the input voltage range of the CS5394/96/97. A nominal input level of 13 Volts rms to the evaluation board will achieve a full scale digital output from the CS5394/96/97. The common mode rejection of the system is limited by the passive component matching of the input buffer circuit. The analog input connector is a standard female XLR with Pin 2 positive, Pin 3 return, and Pin 1 shield.

R1, R5, R16 and C65 form an RC network which provides anti-alias filtering and the optimum source impedance for the CS5394/96/97 right channel inputs. R2, R3, R15 and C66 duplicate this function for the left channel. Notice that this circuit also provides approximately 13.25 dB attenuation to lower the noise contributed from the analog input buffer.

The CS5394/96/97 are able to withstand input currents of 100 mA maximum, as stated in the CS5394 and CS5396/7 data sheets. The OPA627 op-amp is not able to deliver 100 mA, so input protection diodes are not required. However, protection diodes are recommended if there is a possibility that overrange signals could be applied at the ADC inputs which exceed 100 mA. Refer to the Crystal application note, “AN10: A/D Converter Input Protection Techniques.”

CS5394 and CS5396/7 A/D Converters

The CS5394/96/97 A/D converters are shown in Figure 2. A description of these devices is included in the CS5394 and CS5396/7 datasheets.

CS8404A Digital Audio Interface

Figure 4 shows the circuitry for the CS8404A digital audio interface transmitter. The CS8404A can implement AES/EBU, S/PDIF, and EIAJ-340 interface standards. The Digital Interface Format for the transmitter must be set to match the format chosen for the CS5394 or CS5396/7 as defined in Tables 2-4. SW2 provides 8 DIP switches to select various modes and bits for the CS8404A; switch definitions and the default settings for SW2 are listed in Tables 5-6. Digital outputs are provided on an RCA connector via an isolation transformer and on an optical transmitter. For more detailed information on the CS8404A and the digital audio standards, see the CS8403A/CS8404A data sheet.

I/O Port for Clocks and Data

A serial output interface is provided on I/O Port_1, as shown in Figure 6. When I/O Port is set to the MASTER position, MCLK, SCLK, LRCK and SDATA are outputs from I/O Port. When I/O Port is in the SLAVE position, MCLK and SDATA are outputs, while SCLK and LRCK become inputs. Hence, in SLAVE mode, the SCLK and LRCK signals must be externally derived from MCLK to run the ADC. All signals are buffered in order to isolate the converter from external circuitry. Note that the

CS5394/96/97 must also be properly configured for Slave or Master mode.

CS8404A Format Configuration

The CS5394/96/97 supports two Digital Interface Formats for both master and slave configurations. Format 0 has valid data on the rising edge of SCLK and the CS8404A has no corresponding mode. However, inverting SCLK so that data is valid on the falling edge of SCLK will make Format 0 of the CS5394/96/97 match Format 1 of the CS8404A. Jumpers are available to configure the CS8404A to Format 1 and perform inversion of SCLK. See Tables 4-6.

Digital Interface Format 1 is the I2S compatible mode and matches Format 4 of the transmitter. Refer to Tables 4-6 for jumper positions.

CS8404A MCLK Generation

The crystal oscillator (U5) is either 256x for the 64x oversampling mode or 512x for the 128x oversampling mode. However, the CS8404A requires a master clock frequency of 128x Fs. Therefore, the MCLK must be divided by either 2 or 4 depending on the mode of operation. Refer to Tables 4-6 for the proper jumper selection.

Grounding and Power Supply Decoupling

The CS5394/96/97 require careful attention to power supply and grounding arrangements to optimize performance. The CS5394/96/97 is positioned over the analog ground plane.

This layout technique is used to minimize digital noise and to insure proper power supply matching/sequencing. The decoupling capacitors are located as close to the ADC as possible. Extensive use of ground plane fill on both the analog and digital sections of the evaluation board yields large reductions in radiated noise effects.

The evaluation board uses separate analog and digital ground planes which are joined at the converter. This arrangement isolates the analog circuitry from the digital logic.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5VA	input	+5 Volts for analog section
+5VD	input	+5 Volts for digital section
±12V	input	±12 Volts for analog input
AGND	input	Analog ground connection from power source
DGND	input	Digital ground connection from power source
AINL	input	Left channel differential/single ended analog input
AINR	input	Right channel differential/single ended analog input
LRCK, SCLK	input/output	I/O for serial and left/right clocks
MCLK	output	Master clock output
SDATA	output	Serial data output
coaxial output	output	CS8404A digital output via transformer
optical output	output	CS8404A digital output via optical transmitter

Table 1. System Connections

Jumper	Purpose	Position	Function Selected
HDR1	Sets the proper pull-up for the parallel port	**High** Low	Selects a 2k pull-up for I2C compliance Invalid selection for uC mode
HDR7	Sets the proper pull-up for the parallel port	**High** Low	Selects a 2k pull-up for I2C compliance Invalid selection for uC mode
HDR8	Sets the proper pull-up for the parallel port	**High** Low	Selects a 2k pull-up for I2C compliance Invalid selection for Control Port mode
HDR10	Selects Stand-Alone or Control Port mode	**High** Low	Selects Control Port Mode Invalid selection for Control Port Mode
HDR11	Selects I2C or SPI mode for CS5396/97 control port	**High** Low	Selects I2C mode Selects SPI Mode
SDATA	Selection of data source for output from the SPDIF and I/O port	1 2	Selects SDATA1 Selects SDATA2
I/O Port	I/O port Slave or Master selection	Slave **Master**	LRCK and SDATA are inputs to the port. LRCK and SDATA are outputs from the port
8404A Mode 1 Mode 2 Mode 3	Sets CS8404A data format selection for CS5396/97 compatibility. All jumpers must be set to either I2S or LJ and be compatible with the CS5396/97 data format.	**I2S** LJ	I2S data format selected Left Justified data format selected
CS8404A	MCLK divide for CS8404 and CS5396/97 compatibility	**128 x** 64 x	Divide MCLK by 4 for 128x oversampling mode Divide MCLK by 2 for 64x oversampling mode
CS5396/97	Supports a future function of the CS5396/97	High Low	Invalid selection Should be set LOW

Bold indicates default settings

Table 2. CDB5396 and CDB5397 Control Port Mode jumper Setting

Jumper	Purpose	Position	Function Selected
HDR1	Secondary effect on power-down implementation	High **Low**	Invalid selection for Stand-alone Mode Must be set low for operation
HDR7	CS5396/97 digital data format selection	**High** Low	Selects I2S data format Selects Left justified data format
HDR8	CS5396/97 Master or Slave mode selection	High **Low**	Selects Slave Mode Selects Master Mode
HDR10	Selects Stand-alone or Control Port mode	High **Low**	Selects Control Port Mode Selects Stand-alone Mode
HDR11	Selects polarity of power-down	**High** Low	Must be set High Invalid selection, CDB will not function
SDATA	Selection of Data source for output from the SPDIF and I/O port	1 2	Selects SDATA1 Selects SDATA2
I/O Port	I/O port Slave or Master selection	Slave **Master**	LRCK and SDATA are inputs to the port LRCK and SDATA are outputs from the port
8404A Mode 1 Mode 2 Mode 3	Sets CS8404A data format selection for CS5396/97 compatibility. All jumpers must be set to either I2S or LJ and be compatible with the CS5396/97 data format (HDR7)	**I2S** LJ	I2S data format selected Left Justified data format selected
CS8404A	MCLK divide for CS8404 and CS5396/97 compatibility	128 x **64 x**	Divide MCLK by 4 for 128x oversampling mode Divide MCLK by 2 for 64x oversampling mode
CS5396/97	Supports a future function of the CS5396/97	High Low	Invalid selection Should be set LOW

Table 3. CDB5396 and CDB5397 Stand-Alone Mode Jumper Settings

Jumper	Purpose	Position	Function Selected
HDR1	Secondary effect on power-down implementation	High **Low**	Invalid selection for Stand-alone Mode Must be set low for operation
HDR7	CS5394 digital data format selection	**High** Low	Selects I2S data format Selects Left justified data format
HDR8	CS5394 Master or Slave mode selection	High **Low**	Selects Slave Mode Selects Master Mode
HDR10	Selects Stand-alone or Control Port mode	High **Low**	Invalid selection for CS5394 Selects Stand-alone Mode
HDR11	Selects polarity of power-down	**High** Low	Must be set High Invalid selection, CDB will not function
SDATA	Selection of Data source for output from the SPDIF and I/O port	1 2	Selects SDATA1 Invalid selection for CS5394
I/O Port	I/O port Slave or Master selection	Slave **Master**	LRCK and SDATA are inputs to the port LRCK and SDATA are outputs from the port
8404A Mode 1 Mode 2 Mode 3	Sets CS8404A data format selection for CS5394 compatibility. All jumpers must be set to either I2S or LJ and be compatible with the CS5394 data format (HDR7)	**I2S** LJ	I2S data format selected Left Justified data format selected
CS8404A	MCLK divide for CS8404 and CS5394 compatibility	128 x **64 x**	Invalid selection for CS5394 Divide MCLK by 2 for 64x oversampling mode
CS5396/97	Supports a future function of the CS5396/97	High Low	Invalid selection Should be set LOW

Bold indicates default settings

Table 4. CDB5394 Jumper Settings

Switch#	0=Closed, 1=Open	Comment
6	$\overline{PRO=0}$	Consumer Mode (C0=0)
	FC1, FC0	C24,C25,C26,C27 - Sample Frequency
8, 5	0 0 *0 1 1 0 1 1	0000 - 44.1 kHz 0100 - 48 kHz 1100 - 32 kHz 0000 - 44.1 kHz, CD Mode
7	$\overline{C3}$	C3,C4,C5 - Emphasis (1 of 3 bits)
	*1 0	000 - None 100 - 50/15 µs
4	$\overline{C2}$	C2 - Copy/Copyright
	*1 0	0 - Copy Inhibited/Copyright Asserted 1 - Copy Permitted/Copyright Not Asserted
3	$\overline{C15}$	C15 - Generation Status
	*1 0	0 - Definition is based on category code 1 - See CS8402A Data Sheet, App. A
	$\overline{C8}$, $\overline{C9}$	C8-C14 - Category Code (2 of 7 bits)
1, 2	1 1 1 0 0 1 *0 0	0000000 - General 0100000 - PCM encoder/decoder 1000000 - Compact Disk - CD 1100000 - Digital Audio Tape - DAT

Table 5. CS8404A Switch Definitions - Consumer Mode

Switch#	0=Closed, 1=Open	Comment
6	$\overline{PRO=1}$	Professional Mode (C0=1)
8	CRE	Local Sample Address Counter & Reliability Flags
	0 1	Disabled Internally Generated
7, 4	$\overline{C6}$, $\overline{C7}$	C6,C7 - Sample Frequency
	1 1 1 0 0 1 0 0	00 - Not Indicated - Default to 48 kHz 01 - 48 kHz 10 - 44.1 kHz 11 - 32 kHz
5	$\overline{C1}$	C1 - Audio
	1 0	0 - Normal Audio 1 - Non-Audio
3	$\overline{C9}$	C8,C9,C10,C11 - Channel Mode (1 of 4 bits)
	1 0	0000 - Not indicated - Default to 2-channel 0100 - Stereophonic
1, 2	EM1, EM0	C2,C3,C4 - Emphasis (2 of 3 bits)
	1 1 1 0 0 1 0 0	000 - Not Indicated - Default to none 100 - No Emphasis 110 - 50/15 µs 111 - CCITT J.17

Table 6. CS8404A Switch Definitions - Professional Mode

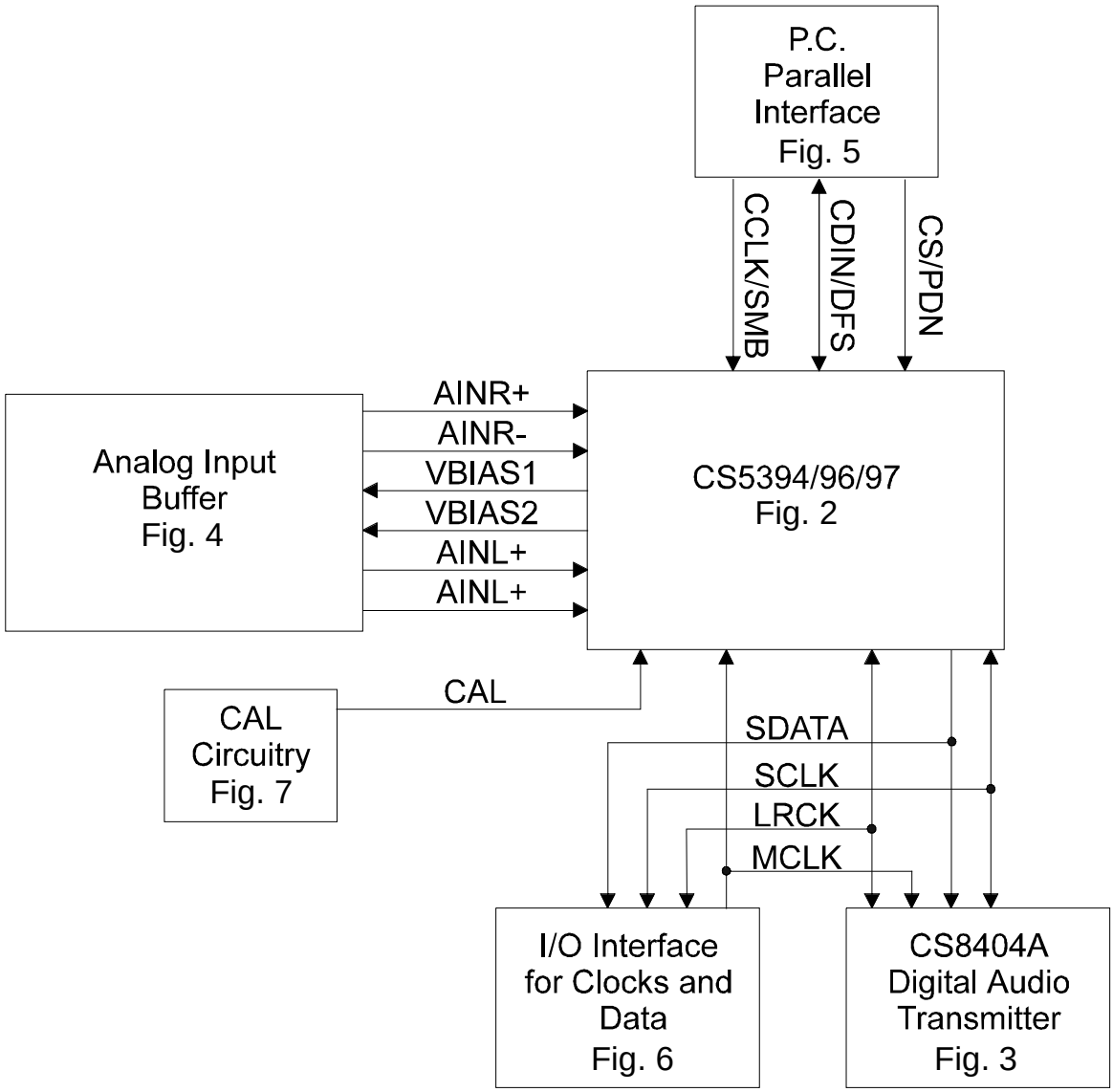


Figure 1. System Block Diagram and Signal Flow

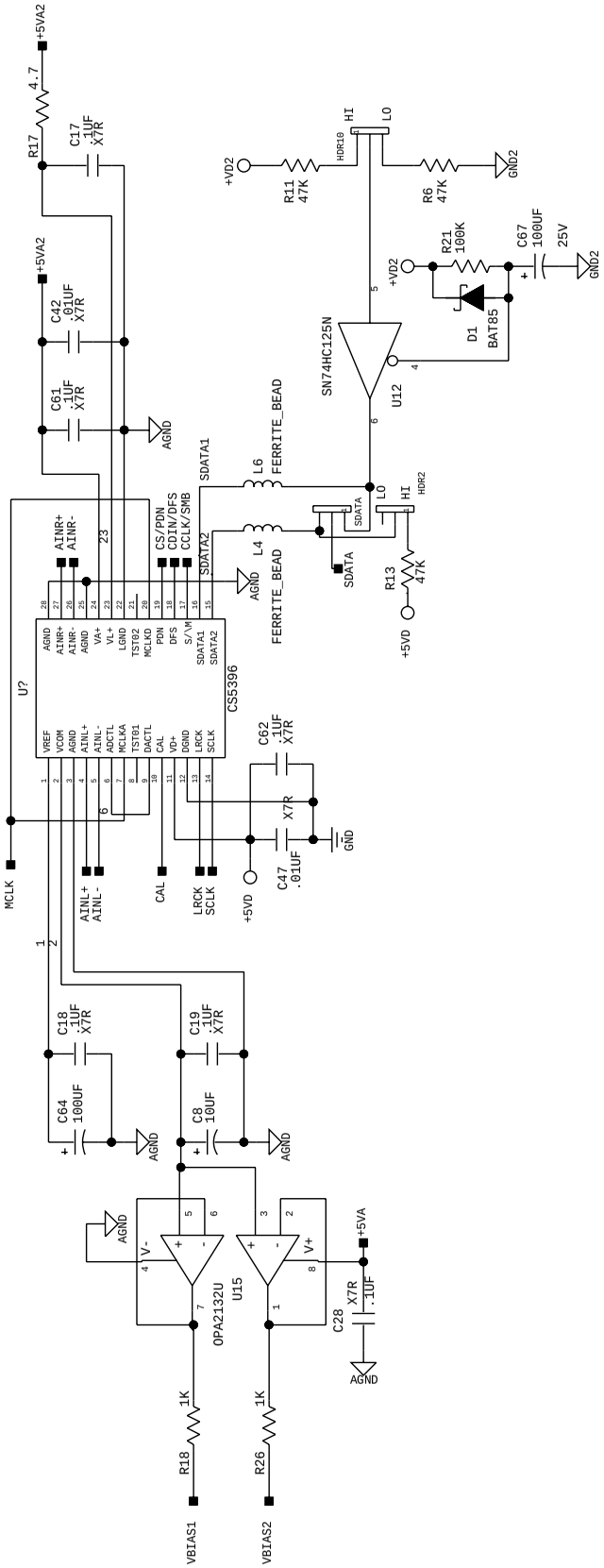


Figure 2. CS5394 and CS5396/7 Connections

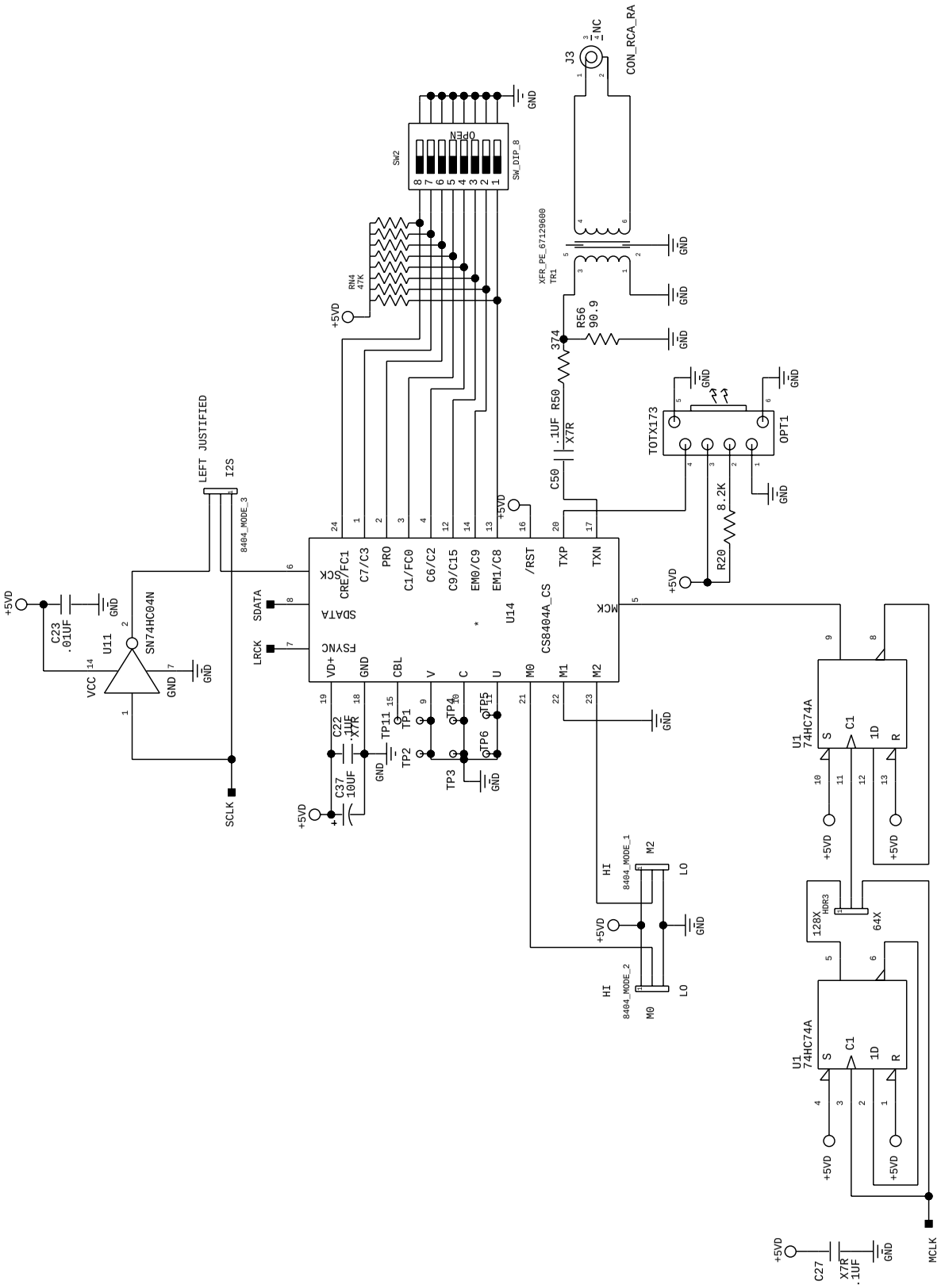


Figure 3. CS8404A Digital Audio Transmitter and Connections

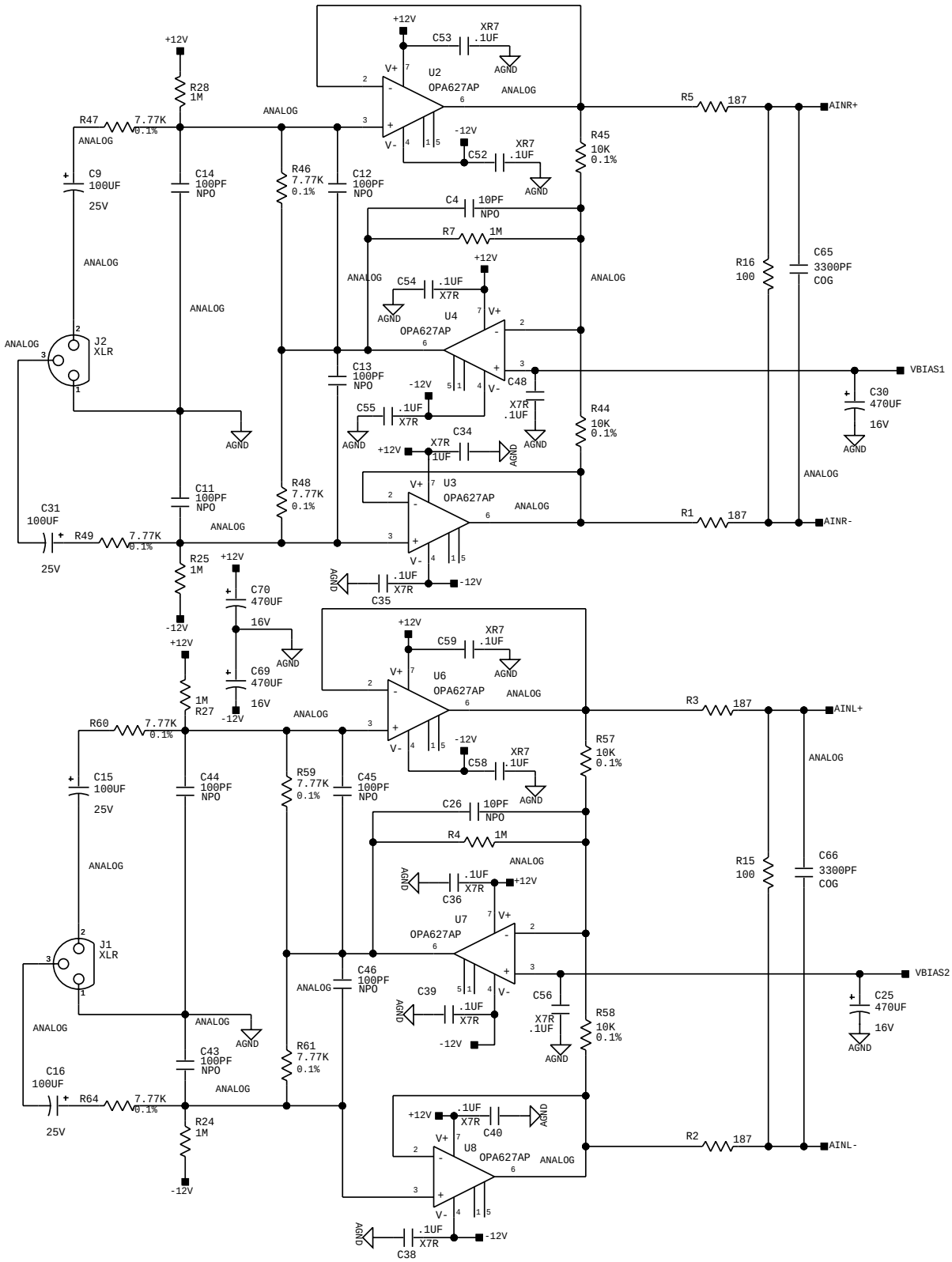


Figure 4. Analog Input Buffer

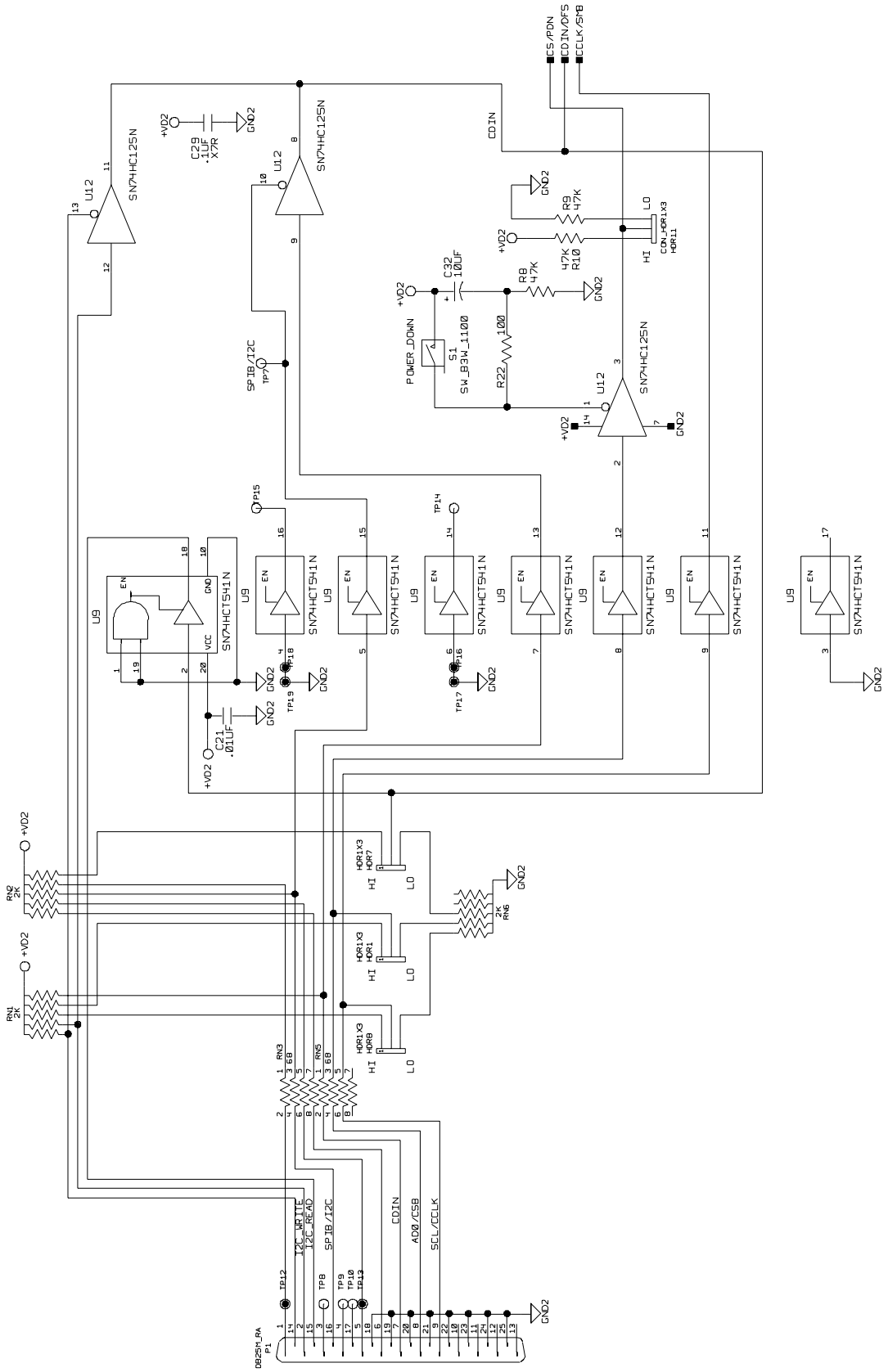


Figure 5. P.C. Parallel Interface

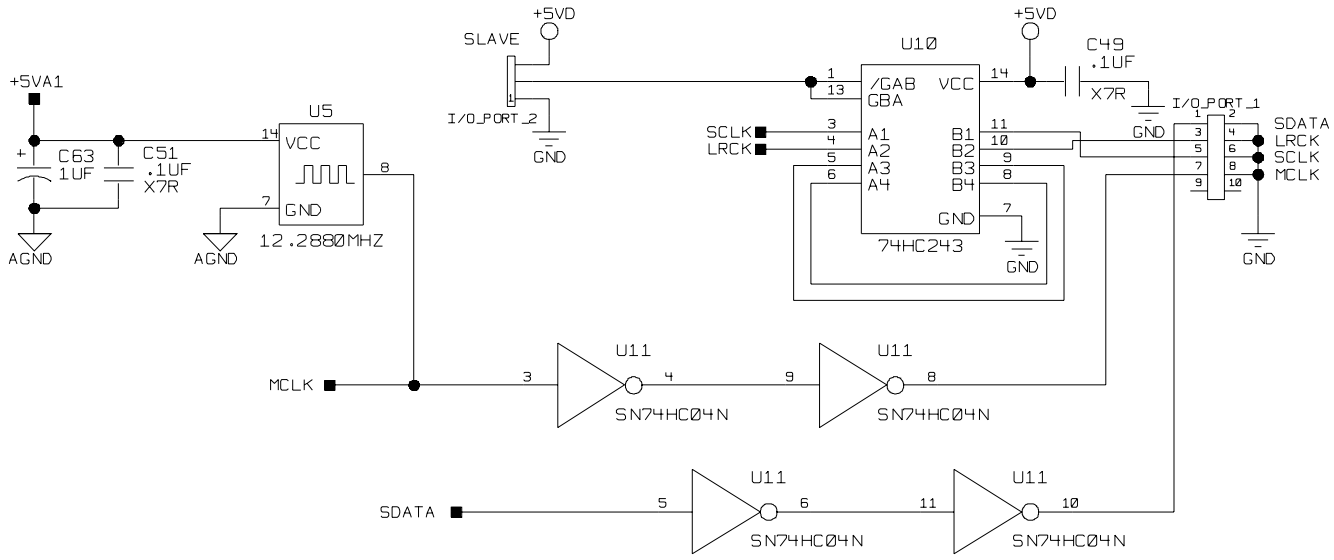


Figure 6. I/O Interface for Clocks & Data

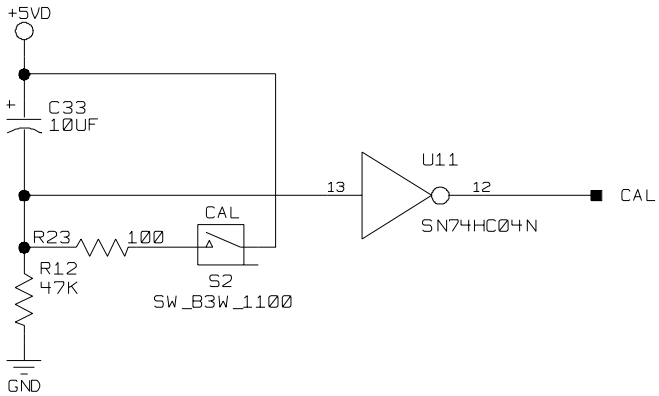


Figure 7. CAL Circuitry

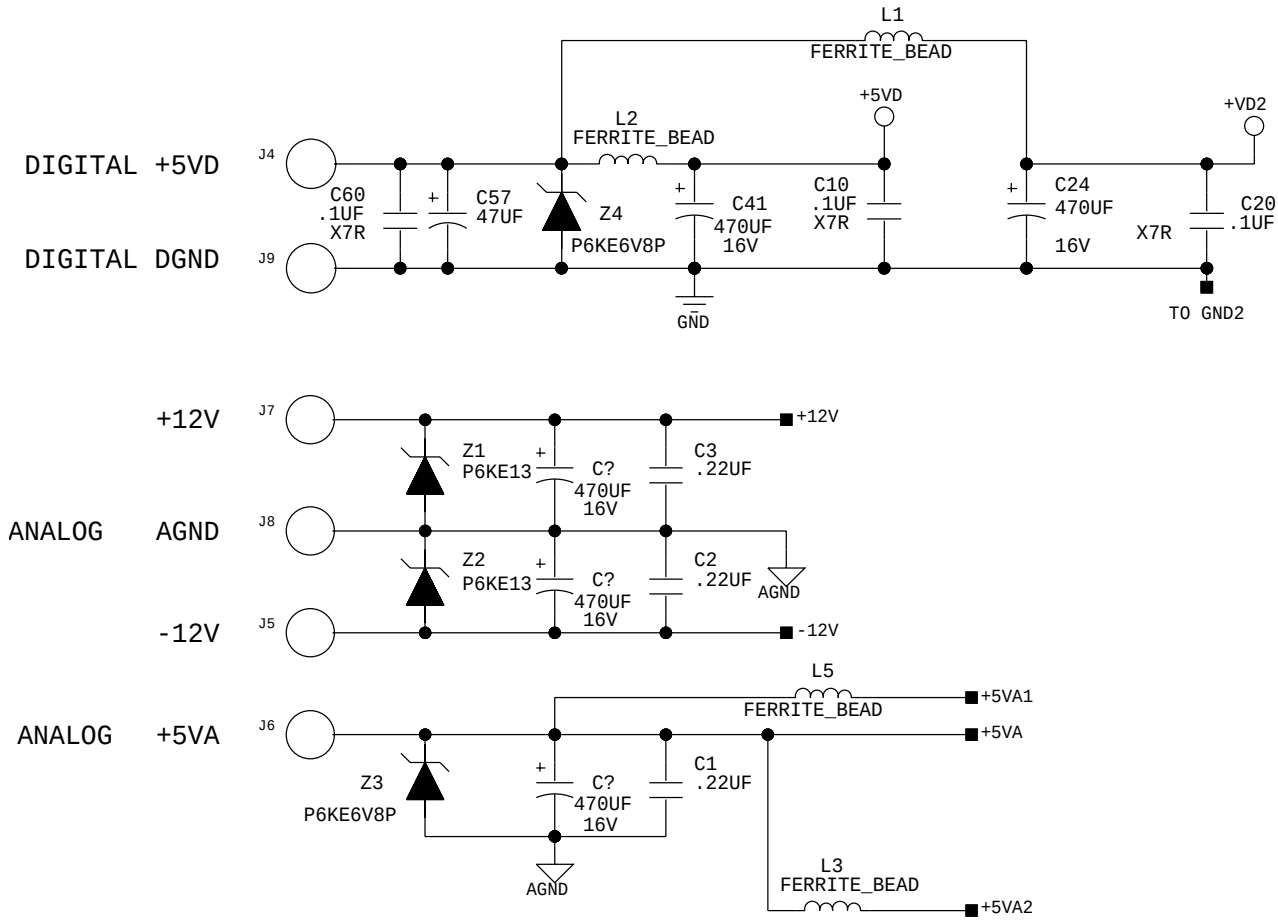


Figure 8. Power Supply & Reset Circuitry

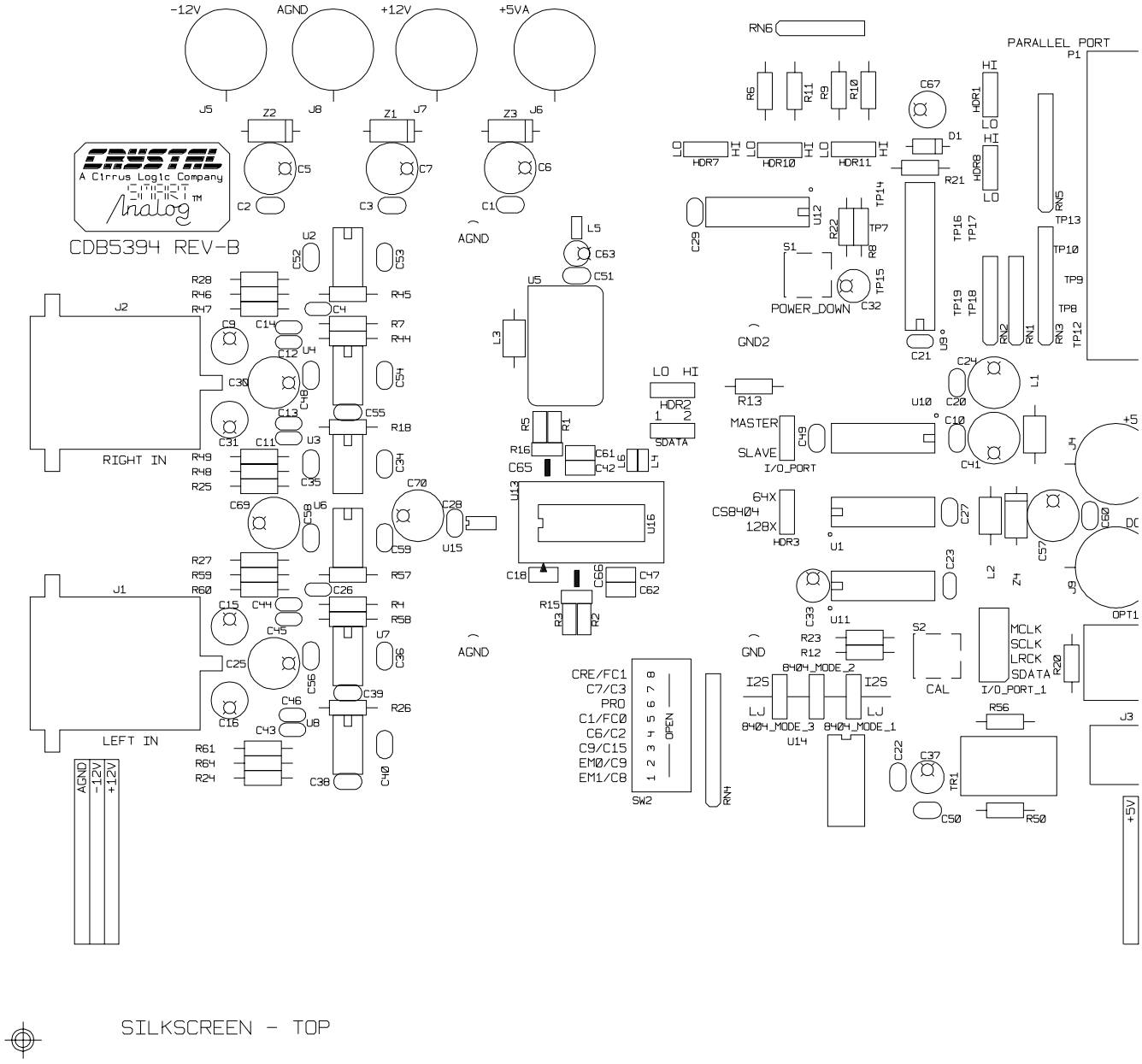


Figure 9. CDB5394 and CDB5396/7 Component Silkscreen Side (top)

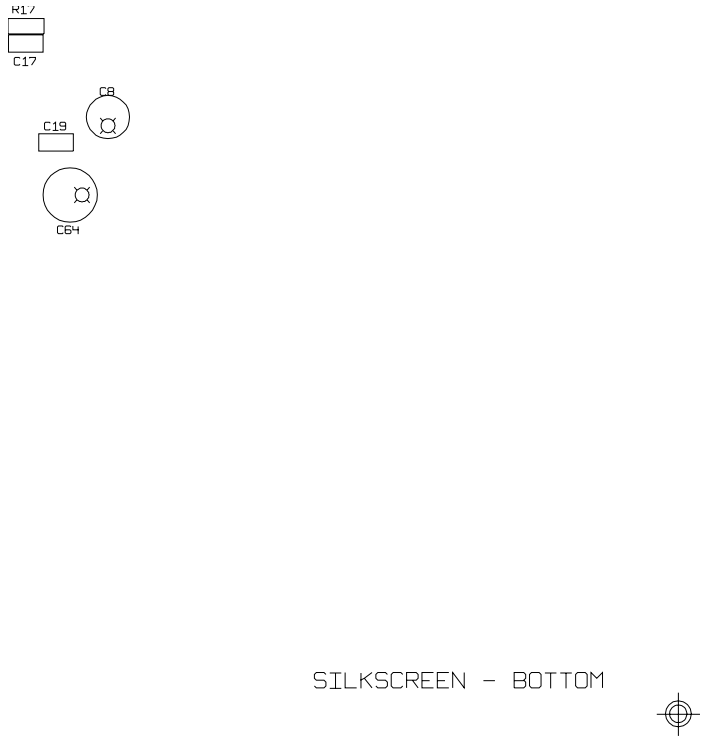
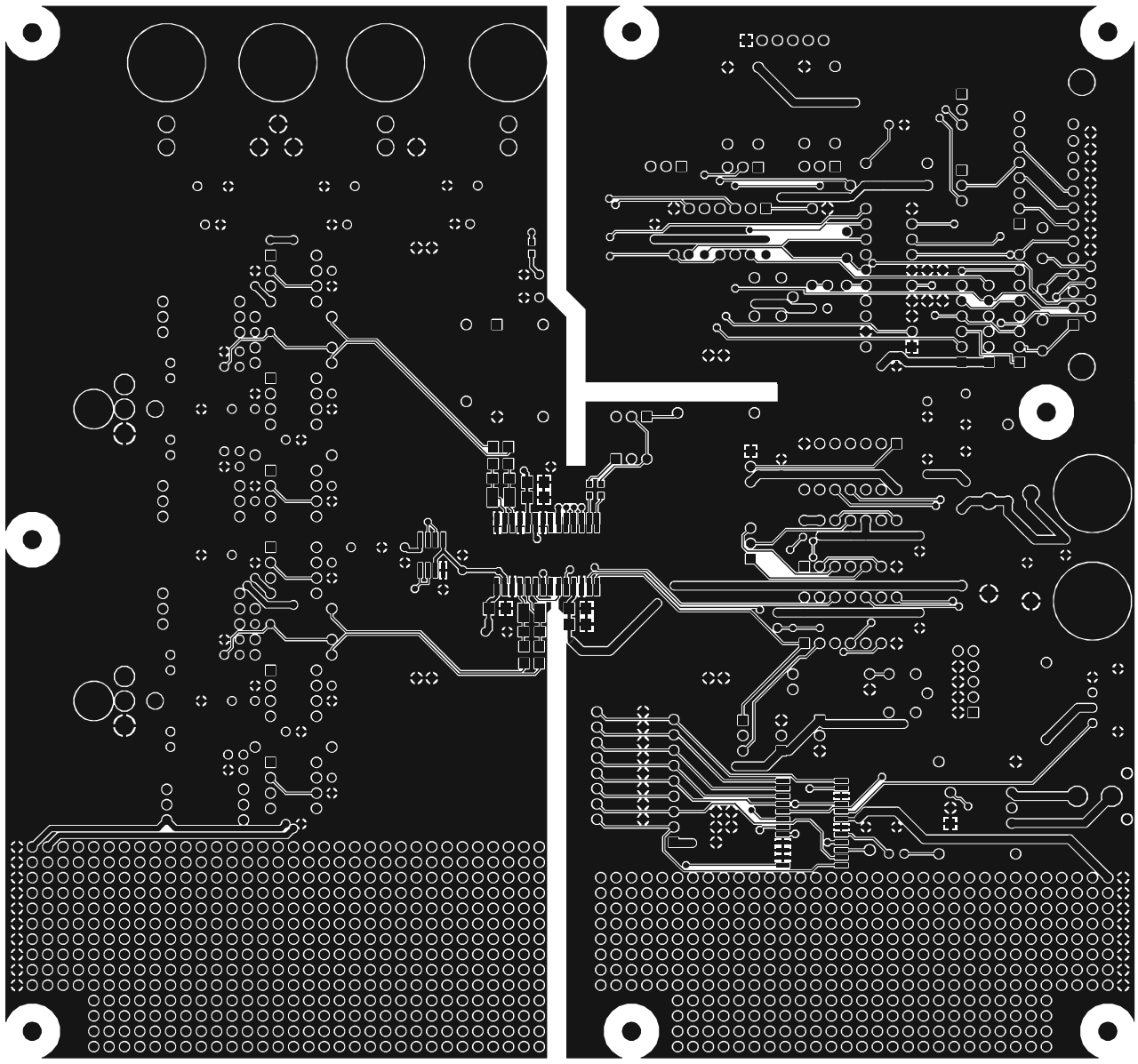
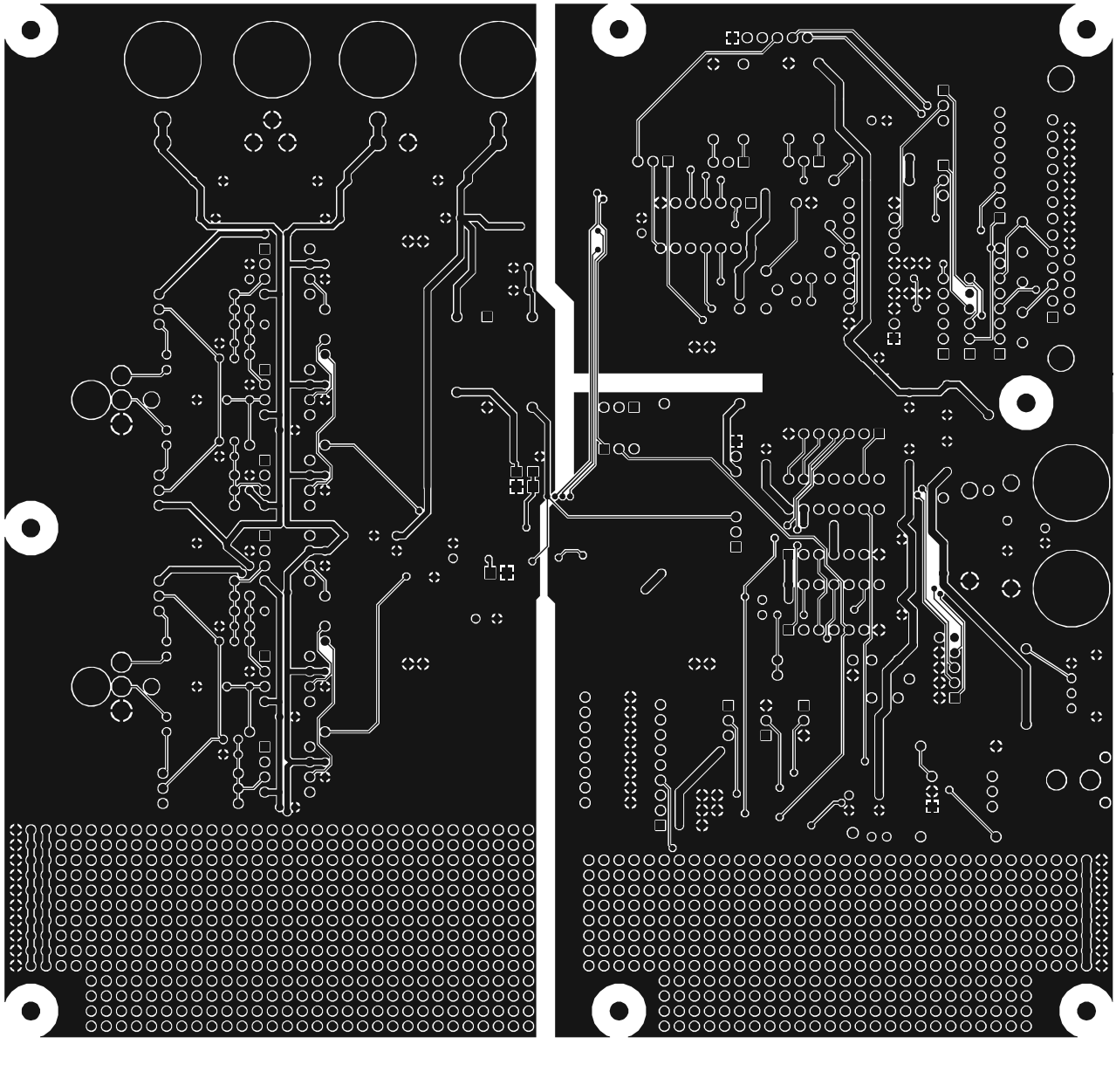


Figure 10. CDB5394 and CDB5396/7 Component Silkscreen Side (bottom)



TOP SIDE

Figure 11. CDB5394 and CDB5396/7 Component Copper Side (top)



BOTTOM SIDE

Figure 12. CDB5394 and CDB5396/7 Component Copper Side (bottom)

• Notes •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